IPC/NETIPC-4A(E), -4AD(E)

Document Ordercode: DOC/IPC_NETIPC4-E

Revision	Date	Author	Modification
1.0	09.03.2010	U. Müller	first release

Contents

List of Tables

List of Figures

1 Introduction

1.1. General Remarks

The content and presentation of this document has been carefully checked. No responsibility is accepted for any errors or omissions in the documentation.
Note that the documentation for the products is constantly revised and improved. The right to change this documentation at any time without notice is therefore reserved.
Syslogic is grateful for any help referring to errors or for suggestions for improvements.
The following registered trademarks are used:

IBM-PC, PC/AT, PS/2	trademarks of IBM Corporation
I^2C	trademark of Philips Corporation
CompactFlash	trademark of SanDisk Corporation
DiskOnChip	registered trademark of M-Systems LTD
PC/104	trademark of PC/104 Consortium
FBCube, EUROLOG	trademarks of Syslogic Datentechnik AG

1.2. Contents of this Documentation

This document addresses to system integrators, programmers and instructed installation and maintenance personal working with the PC/104 system. It provides all information needed to configure, setup and program the IPC/NETIPC-4A, -4AD processor boards. For complete information also the documentation of the mounted communications and I/O boards must be consulted. In the following paragraphs all descriptions referenced to NETIPC apply to all, the IPC/NETIPC-4A, -4AD products, if not declared otherwise.

1.3. Additional Products and Documents

1.3.1. Hardware Products

The following hardware products are useful together with the NETIPC processor board:
- NETIPC boot loader key (BOOTPLUG-1A, part of CUB/DOWNKIT-1A)
- NETIPC serial port cable (AT-Link cable, part of CUB/DOWNKIT-1A)
- PC/104 communication boards (see product catalog)
- PC/104 I/O boards (see product catalog)

1.3.2. Software Products

The following software products are useful together with the NETIPC processor board:
- IPC/NETIPCFW-1A: Firmware for NETIPC boards
- IPC/IOCOMSW-1A: Sample program code and utilities for x86 based PC/104 systems

1.3.3. Documents

The following documents are *required* for correct installation and operation of the NETIPC processor board:

- DOC/CASE19: User Documentation for IPC Enclosure and Installation
  Note : also contains the necessary information related to the “ce”-certification of the products
- DOC/NETIPCFW: User Documentation for NETIPC Firmware
- DOC/IPC_IOCOMSW: User Documentation for programming examples and utilities

The following documents are *useful* for additional information about PC/104 and IEEE 996.1:

- PC/104 Specification Version 2.3
- IEEE 996: IEEE standard document ‘Personal Computer Bus Standard’
- IEEE 996.1: IEEE standard document ‘Compact Embedded-PC Modules’
- ISBN 0-929392-15-9: ‘ISA & EISA, Theory and Operation’ by Edward Solari (Annabooks, San Diego)

The PC/104 Specification may be downloaded from the Internet (see address below).

- PC/104 Consortium
  www.pc104.org

The IEEE standard documents may be ordered directly from the IEEE or any standards document distributor (see addresses below).

- IEEE Standards Department
  www.ieee.org
- Global Engineering Documents
  www.global.ihs.com

1.4. Items delivered

The NETIPC comes without cabling and enclosure. These additional items must be ordered separately and installed according to the respective user documentations. A standard configuration based on the NETIPC processor board could be as follows:

- PC/104 power supply board
- PC/104 processor board IPC/NETIPC-4AE
- enclosure
- Cabling for two serial ports and mouse port
  Note : Mounting procedure is described in DOC/CASE19

1.5. Installation

The installation of the NETIPC board is described in the documentation DOC/CASE19.
The firmware configuration and download is described in the appropriate firmware documentation.

Important Note

Before applying power to the NETIPC system, all installed boards must be correctly configured and mounted (please consult corresponding User Documentations).

1.6. Safety Recommendations and Warnings

The products are intended for measurement, control and communications applications in industrial environments. The products must be assembled and installed by specially trained people. The strict observation of the assembly and installation guidelines is mandatory.
The use of the products in systems in which life or health of persons is directly dependent (e.g. life support systems, patient monitoring systems, etc.) is not allowed.
The use of the products in potentially explosive atmospheres requires additional external protection circuitry which is not provided with the products.
In case of uncertainty or of believed errors in the documentation please immediately contact the manufacturer (address see chapter 8). Do not use or install the products if you are in doubt.
In any case of misuse of the products, the user is solely liable for the consequences.

1.7. Life Cycle Information

1.7.1. Transportation and Storage

During transportation and storage the products must be in their original packing. The original packing contains an antistatic bag and shock-absorbing material. It is recommended, to keep the original packing in case of return of the product to the factory for repair. Note that the packing is recyclable.

1.7.2. Assembly and Installation

Observe the EMI-precautions against static discharge. Carefully read the assembly and installation documentation (Document DOC/CASE19) before unpacking the products. Make sure that you have all the necessary items ready (including all the small parts). Follow the assembly guidelines in DOC/CASE19 strictly.
The installation procedures (contained in document DOC/CASE19) must be strictly observed. Note that deviations from the installation guidelines may result in degraded operational reliability or in unfavourable EM-radiation or EM-susceptibility.

1.7.3. Operation

The operating environment must guarantee the environmental parameters (temperature, power supply, etc.) specified in the technical specification section of the product manuals.
The main functionality of the IPC system is defined by the application programs running on the processor board. The application programs are not part of the delivery by Syslogic but are defined, developped and tested by the customer or a system-integrator for each specific application. Refer to the respective documentation for more information.

1.7.4. Maintenance and Repair

The IPC system features error- and malfunction-detection circuitry. Diagnostic information gathered is transferred to the applications software where it can be used. In the rare case of a module hardware-failure or malfunction, the complete board should be exchanged. The faulty board must be returned to the factory for repair. Please use whenever possible the original packing for return of the product (EMI and mechanical protection).

1.7.5. Disposal

At the end of the lifespan the IPC products must be properly disposed. IPC products contain a multitude of elements and must be disposed like computer parts. Some of the IPC products contain batteries which should be properly disposed.

2 Product Description

2.1. Features

The NETIPC board is x86 based processor board designed for use with the IPC line of communications and I/O boards. Using the same form factor, it fits in all standard IPC enclosures to build up various industrial controls based on the standard PC/AT architecture.
The NETIPC offers the following main features:

- low power industrial processor board eliminating the need for enforced cooling
- high performance 32-bit 6-stage pipeline x86 based processor core with integrated floating point unit
- 600..800 MHz processor clock
- DDR2 DRAM interface
- 256 Mbyte DRAM on board
- 64-bit graphics controller with backwards compatibility to VGA and SVGA standards (not available on NETIPC-4AD)
- CRT controller supporting up to 1280 x 1024 dots resolution at 75 Hz (not available on NETIPC-4AD)
- LCD interface (3x6 bit CMOS)
- Enhanced IDE interface supporting 2 IDE devices with PIO modes 0..4 and Ultra-DMA 100.
- standard 44 pin 2mm IDE connector for two external IDE devices
- CompactFlash Type I connector for onboard mountable CompactFlash card configurable as master or slave IDE device (replacing one of the external IDE devices)
- integrated peripheral controller (IPC) with PC/AT compatible DMA controllers (2 x 8237), interrupt controllers (2 x 8259) and timer/counter channels (8254)
- PC/AT compatible keyboard controller (8042) with PS/2 mouse support
- Two serial RS232 ports (COM1, COM2) with 16 byte receive and transmit fifo (16550A)
- Two USB V2.0 ports (OHCI/EHCI-Hostcontroller) with High-, Full- and Low-Speed support
- 10/100Mbit Ethernet interface
- Year 2000 compliant Real Time Clock (PC/AT compatible)
- hardware watchdog configurable for 100 ms or 1.6 s timeout and Non-maskable Interrupt (NMI) or hardware reset activation
- temperatur supervisor for software controlled power management
- 16 Mbit BootBlock Flash for BIOS, BIOS extensions and 1.44 Mbyte ROM-drive A: (floppy replacement)
- 32 pin DIL socket for user installable Socket Memory supporting various types of 32 and 28 pin SRAM, Flash and EEPROM devices from 32 kbyte up to 512 kbyte and supporting DiskOnChip 2000 and DiskOnChip Millennium products

- supervised battery backup for Real Time Clock and Socket Memory through VBat pin on a PC/104 bus extension
- PC/104 bus interface for expansion with standard 8/16 bit PC/104 communications and I/O boards

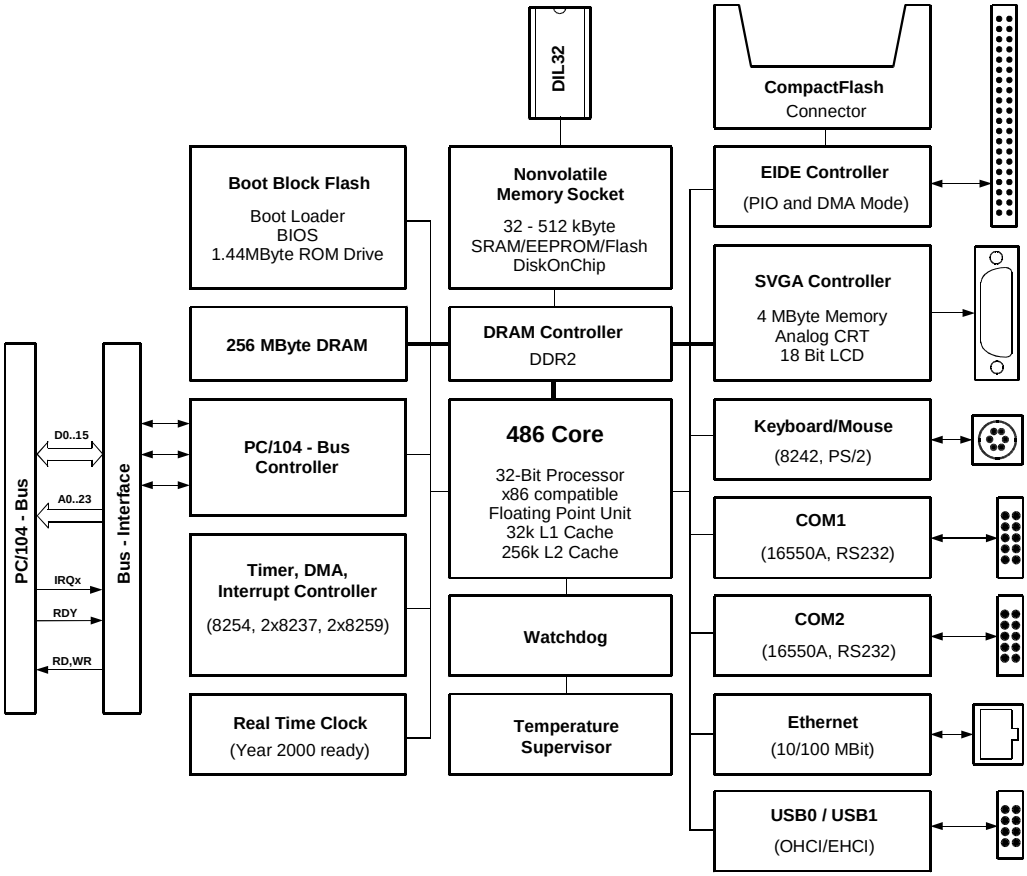

Fig. 1 Block Diagram (NETIPC-4A)

2.2. Operating Modes

The NETIPC is based on the standard PC/AT architecture and therefore operates in DOS-compatible mode (real mode) on start up. The configurable BIOS initializes all onboard peripherals to theire default values, executes the BIOS extensions programmed into the onboard BootBlockFlash by the user and BIOS extensions found on installed expansion boards prior to booting the operating system from a user-selectable drive (boot sector or OS image file). The operating system (or eventually a BIOS extension) may switch to protected mode to execute high performance 32-bit program code.

2.3. Startup Modes

The NETIPC may startup either in normal operating mode or in Boot Loader mode:

- Boot Loader mode is invoked when plugging a special Boot Loader Key into the keyboard connector. In Boot Loader mode the content of the BootBlockFlash (BIOS, BIOS extensions and ROM-drive) may be updated.
- Normal operating mode is invoked when a standard PS/2 keyboard or no keyboard is plugged into the keyboard connector.

3 Hardware Description

3.1. Overview

The NETIPC board hardware may be configured by software (CMOS setup or BIOS configuration program) and by jumper setting. Custom BIOS configuration should be done using a BIOS configuration tool, unless the BIOS does not support it (ask Syslogic technical support for custom BIOS configuration).
The jumper and connector locations are shown in the board layout drawing (Fig. 2).

Important Note

Always check the jumper configuration of a freshly received board to comply with your system requirements before applying power, otherwise the system may get damaged or may fail to operate.

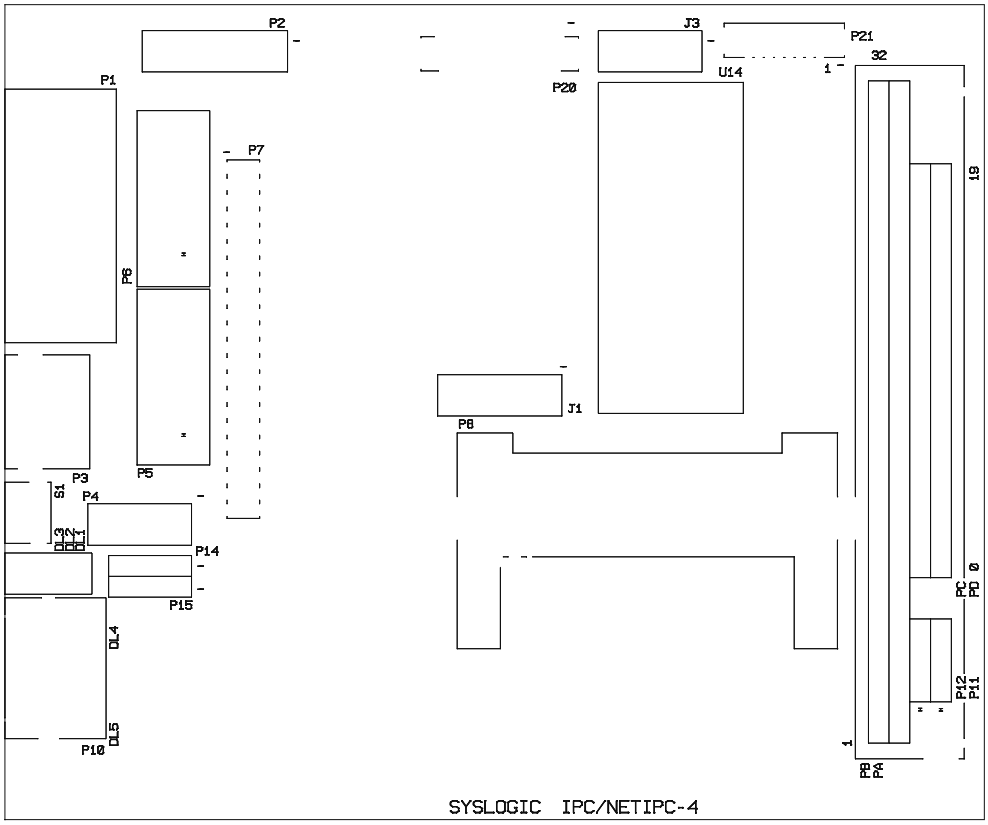

Fig. 2 Board Layout (NETIPC-4A)

3.2. Memory and I/O Resources

3.2.1. General Memory Layout and Configuration

The NETIPC uses the same memory layout as a standard desktop PC. Four onboard devices , DRAM, graphics controller, BootBlockFlash and Socket Memory, make use of the 4 Gbyte adressable memory space.

Address	Device / Register	Remarks
0000'0000..0009'FFFFH	640 kbyte Main Memory (DRAM)	
000A'0000..000B'FFFFH	Video Memory	
000C'0000..000F'FFFFH	Configurable memory range (BIOS, BIOS Extensions, DRAM, Socket Memory or redirected to PC/104 bus)	see paragraph 3.3.1 and 4.2.3
0010'0000..0FFF'FFFFH	255 Mbyte Main Memory (DRAM)	
1000'0000..807F'FFFFH	reserved	do not access
8080'0000..8087'FFFFH	Socket Memory	
8088'0000..83EF'FFFFH	reserved	do not access
83E0'0000..83FF'FFFFH	2 Mbyte BootBlock Flash	
8400'0000..FFFF'FFFFH	reserved	do not access

Tab. 1 Physical Memory Address Space Layout

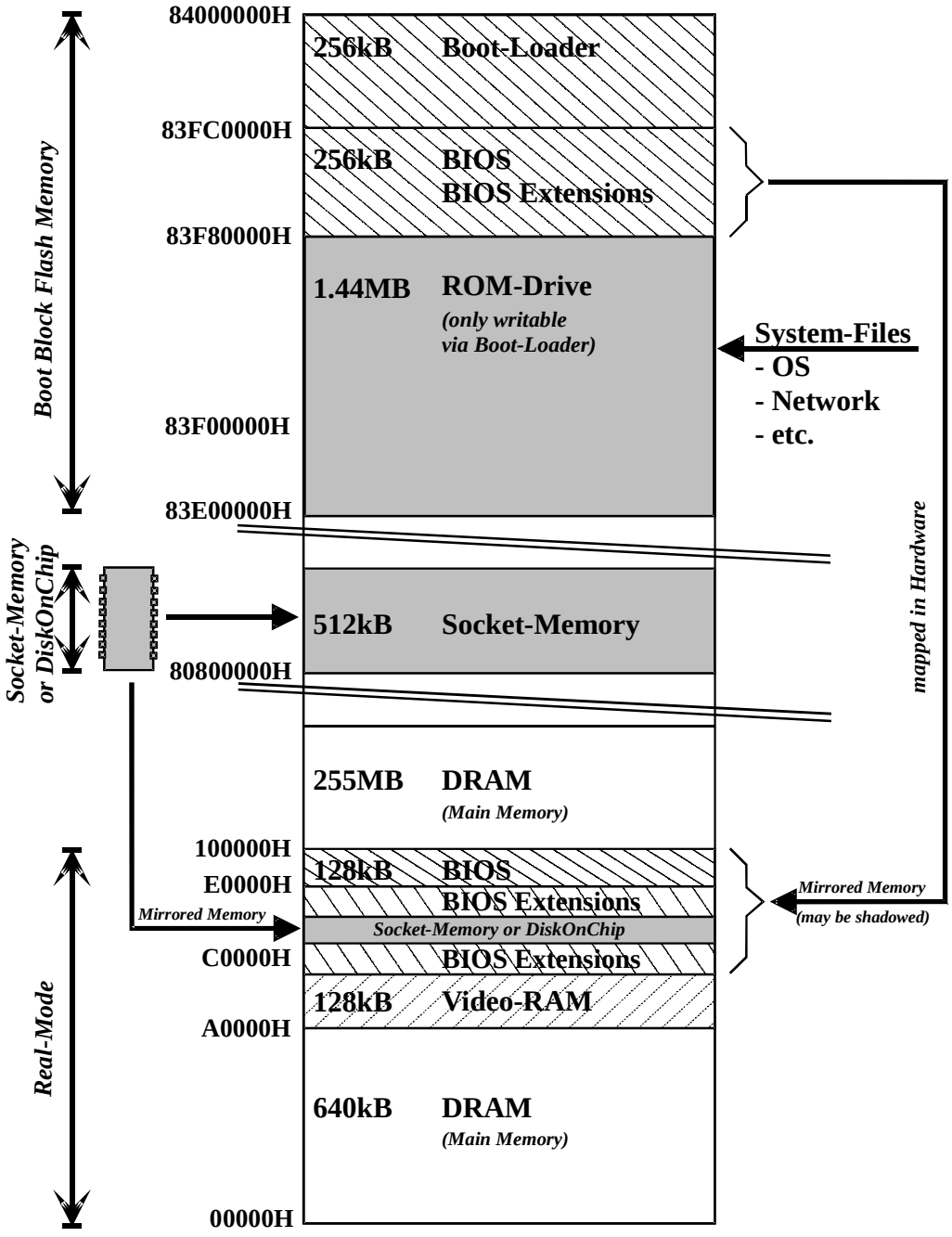

Fig. 3 Memory Map

3.2.2. General I/O Layout and Configuration

The NETIPC's 64 kbyte I/O address space is mapped to the PC/104 bus address space as indicated in the table below. Note that 16 bit address decoding should be used on all PC/104 expansion boards to make efficient use of the I/O address space.

Address	Device / Register	Remarks
0000..001FH	DMA Controller 1	
0020..0021H	Master Interrupt Controller	
0022H	Configuration Address Register	
0023H	Configuration Data Register	
0024..003FH	reserved	
0040..0043H	Timer/Counter	
0044..005FH	reserved	
0060H	Keyboard/Mouse Controller	
0061H	Port B Register	
0062..0063H	reserved	
0064H	Keyboard/Mouse Controller	
0065..006FH	reserved	
0070H	Bit 6..0 = RealTimeClock/CMOS-RAM Address Register Bit 7 = Non Maskable Interrupt (NMI) Mask (write only)	
0071H	RealTimeClock/CMOS-RAM Data Register	
0072..007FH	reserved	
0080..0091H	DMA Page Registers / reserved	
0092H	Port 92h System Control Register	
0093..009FH	reserved	
00A0..00A1H	Slave Interrupt Controller	
00A2..00BFH	reserved	
00C0..00DFH	DMA Controller 2	
00E0..010FH	reserved	
0110..016FH	not used	
0170..0177H	reserved for external Secondary IDE Channel	
0178..01EFH	not used	
01F0..01F7H	Primary IDE Channel	
01F8..0277H	not used	
0278..027FH	reserved for external Parallel Port (LPT2) and Plug'n Play	
0280..02E7H	not used	
02E8..02EFH	reserved for external Serial Port (COM4)	
02F0..02F7H	not used	
02F8..02FFH	Serial Port (COM2)	
0300..036FH	not used	
0370..0377H	reserved for external Secondary Floppy Controller	
0376..0377H	reserved for external Secondary IDE Channel	
0378..037FH	reserved for external Parallel Port (LPT1)	
0380..03AFH	not used	
03B0..03BBH	VGA registers (MDA)	

03BC..03BFH	reserved for external Parallel Port (LPT3)	
03C0..03CFH	VGA registers (EGA)	
03D0..03DFH	VGA registers (CGA)	
03E0..03E7H	not used	
03E8..03EFH	reserved for external Serial Port (COM3)	
03F0..03F7H	reserved for external Primary Floppy Controller	
03F6..03F7H	Primary IDE Channel	
03F8..03FFH	Serial Port (COM1)	
0400..042FH	reserved	
0430..04EFH	not used	
0480..048FH	DMA High Page Registers / reserved	
0490..049FH	Instruction Counter Registers / reserved	
04A0..04CFH	not used	
04D0..04D1H	IRQ Edge/Level Control	
04D2..04FFH	not used	
0500..08FFH	not used	
0900..0A77H	not used	
0A78H	Plug'n Play configuration port	
0A79..0BFFH	not used	
0C00..0CF7H	not used	
0CF8..0CFFH	PCI configuration registers	
0D00..0FFFH	not used	
1000..3FFFH	not used	
4000.. 46E7H	not used	
46E8H	reserved	
46E9..47FFH	not used	
4800..7FFFH	not used	
8000..81FFH	reserved	
8200..821FH	NETIPC system registers	
8220..83FFH	reserved for Syslogic IPC add-on boards	
8400..BFFFH	reserved	
C000..EFFFH	reserved for PCI devices (VGA, Ethernet, USB, IDE)	
F000..FFFFH	reserved	

Tab. 2 I/O Address Space Layout

The programmable logic devices on the NETIPC board are factory programmed using some pins of the internal header J1. These pins **must not** be connected by the user.

Pin Number	Signal	Pin Number	Signal
1	TCK (do not connect)	2	see Tab. 11
3	TDO (do not connect)	4	GND
5	TMS (do not connect)	6	see Tab. 19
7	TDI (do not connect)	8	see Tab. 6
9	+5V	10	see Tab. 6
11	reserved	12	see Tab. 6

Tab. 3 Factory Programming Header J1 (2x6 pin)

The battery backup supply for the onboard Real Time Clock and SRAM must be connected to connector P11 as follows (also see Tab. 20) :

Pin Number	Signal	Remarks
1	GND	
2	no connection	
3	no connection (KEY)	
4	Vbatt	

Tab. 4 External Battery Connector P11 (1x4 pin)

The user programmable output signals STOP* and TRIGGER* are available on connector P12. The signal levels are TTL compatible with maximum 4 mA sink and 2 mA source output current (also see Tab. 20) :

Pin Number	Signal	Remarks
1	GND	
2	+5V	max. 10 mA
3	TRIGGER*	
4	STOP*	

Tab. 5 User Programmable Output Connector P12 (1x4 pin)

The TRIGGER* signal may be controlled by software or by a hardware timer, e.g. Timer Channel 2 Out (Speaker Drive) . See chapter 4.
A speaker may be connected to this signal if buffered with an external NPN transistor or inverting power driver.

3.3. Peripheral Devices

3.3.1. Socket Memory

The NETIPC features a DIL32 socket for user insertable memory devices like SRAM, NVRAM, EEPROM, Flash and DiskOnChip products. Supported devices and corresponding configuration is listed in the table below, maximum access time allowed is 150 ns for all devices. Note that the Socket Memory base address, size and enabling must also be configured by software (BIOS).

Important Note

Do not insert devices not listed. This could damage the hardware.

Important Note

When inserting a 28 pin device into the 32 pin socket, pin 1 of the 28 pin device must be positioned at pin 3 of the DIL32 socket, otherwise the hardware may get damaged.

Memory Type	Manufacturer and Order Code	J1 Setting (pins 8,9,10,12 only)	J3 Setting
SRAM	**Static RAM (5V)**	**5V, Battery Backup enabled**	
128k x 8	Samsung: K6X1008C2D-DB70 Hitachi: HM628128BLP-7 STMicro: M68AF127BL70B6	8-10	1-3, 2-4, 5-6, 8-10
512k x 8	Samsung: K6T4008C1C-DB70 Hitachi: HM628512BLP-7 Mitsubishi: M5M5408AP-70L	8-10	1-3, 2-4, 5-6, 7-8
NVRAM	**Nonvolatile RAM (5V)**	**5V, Battery Backup disabled**	
32k x 8	ZMD: U637256DC70	9-10	1-3, 2-4, 5-6, 8-10
32k x 8	Simtek: STK16C88-W45	9-10	1-3, 2-4, 5-6, 8-10
NVRAM	**Nonvolatile RAM (3.3V)**	**3.3V, Battery Backup disabled (NETIPC-5A only)**	
128k x 8	Simtek: STK16CA8-W45	10-12	1-3, 2-4, 5-6, 8-10
EEPROM	**EEPROM (5V)**	**5V, Battery Backup disabled**	
32k x 8	Atmel: AT28C256(E)-15PC Catalyst: CAT28C256(H)P-15 Hitachi: HN58C256AP-10 ST: M28256-15BS Xicor: X28C256P-15	9-10	1-3, 2-4, 5-6, 8-10
64k x 8	Catalyst: CAT28C512(H)P-15 SST: SST29EE512A-90-4C-PH Xicor: X28C512P-15	9-10	1-2, 3-5, 4-6, 8-10
128k x 8	Atmel: AT28C010(E)-15PC SST: SST29EE010A-120-4C-PH Xicor: X28C010D-15	9-10	1-2, 3-5, 4-6, 8-10
Flash	**Flash Memory (5V)**	**5V, Battery Backup disabled**	
128k x 8	AMD: Am29F010B-90PC Atmel: AT29C010A-15PC SST: SST39SF010-90-4C-PH	9-10	1-2, 3-5, 4-6, 8-10
512k x 8	AMD: Am29F040B-90PC Atmel: AT29C040A-15PC SST: SST39SF040-90-4C-PH	9-10	1-2, 3-5, 4-6, 7-8
Flash	**Note: PLCC32 to DIL32 socket converter required**	**5V, Battery Backup disabled**	
512k x 8	Fujitsu: MBM29F040C-90PD ST: M29F040-90K1	9-10	1-2, 3-5, 4-6, 7-8
DOC	**DiskOnChip (5V)**	**5V, Battery Backup disabled**	
DiskOnChip 2000	M-Systems: MD2200-Dxx	9-10	1-2, 3-5, 4-6, 8-10
DiskOnChip Millennium	M-Systems: MD2800-Dxx	9-10	1-2, 3-5, 4-6, 8-10

Tab. 6 Socket Memory Configuration

3.3.2. VGA Interface

The VGA signals are available on the High Density DSUB15 connector P1 for direct connection of VGA compatible monitors. The signals are also available on the internal header P2 for special expansion boards that may convert the VGA signals into other display standards (e.g. PAL/NTSC or digital TFT). The controller uses the standard VGA register interface. All configuration is done by software (BIOS, VGA-BIOS).
The VGA Interface is not available on NETIPC-4AD (connectors P1 and P2 not equipped).

Device Connection

Pin Number	Signal	Remarks
1	RED	
2	GREEN	
3	BLUE	
4	-	
5	GND	
6	Analog GND	
7	Analog GND	
8	Analog GND	
9	+5V	not fused
10	GND	
11	-	
12	DDC Data	
13	HSYNC	
14	VSYNC	
15	DDC Clock	

Tab. 7 VGA connector P1 (DSUB15HD)

Pin Number		Signal	Pin Number		Signal
1		reserved	2		reserved
3	1	RED	4	2	GREEN
5	3	BLUE	6	4	GND
7	5	reserved	8	6	GND
9	7	HSYNC	10	8	VSYNC
11	9	DDC Data	12	10	DDC Clock
13		reserved	14		reserved

Tab. 8 VGA internal Header P2 (2x7/2x5 pin)

Important Note

Check the P2 header type (2x7 or 2x5 pin) and signals in table Tab. 8 before connecting anything. The 2x5 pin header is centered in the 2x7 pin layout.

Important Note

Be careful when using the VGA or video signals on expansion boards. Special design and layout precautions must be met for these high speed analog signals.
Maximum cable length allowed for VGA connection is 15 m.
Use high quality VGA cables (with coaxial wires for RGB signals) for maximum EMI protection.

3.3.3. LCD-Interface

The LCD interface is an optional interface for direct connection of an external TFT display. It supports 3.3V 6-bit CMOS TFT panels on connector P20. Direct inverter connection is provided through P21 if power requirement is not to high.
The LCD interface is not available on NETIPC-4AD (connectors P20 and P21 not equipped).
Note that special BIOS-Version might be required for operation of the LCD interface. Contact Syslogic technical support for details.

Device Connection (LCD-Panel)

Mating connector type: Hirose DF9-31S-1V.

Pin Number	Signal	Remarks
1	GND	Ground
2	DCLK	Clock signal for sampling catch data signal
3	HS	Horizontal sync signal
4	VS	Vertical sync signal
5	GND	Ground
6	R0	Red data signal (LSB)
7	R1	Red data signal
8	R2	Red data signal
9	R3	Red data signal
10	R4	Red data signal
11	R5	Red data signal (MSB)
12	GND	Ground
13	G0	Green data signal (LSB)
14	G1	Green data signal
15	G2	Green data signal
16	G3	Green data signal
17	G4	Green data signal
18	G5	Green data signal (MSB)
19	GND	Ground
20	B0	Blue data signal (LSB)
21	B1	Blue data signal
22	B2	Blue data signal
23	B3	Blue data signal
24	B4	Blue data signal
25	B5	Blue data signal (MSB)
26	GND	Ground
27	DEN	Data enable signal
28	VCC_LCD	Power supply 3.3V
29	VCC_LCD	Power supply 3.3V
30	HMODE (S2 Slider 3)	Scan direction control (off=4k7 pullup to 3.3V / on=ground)
31	VMODE (S2 Slider 4)	Scan direction control control (off=4k7 pullup to 3.3V / on=ground)

Tab. 9 LCD connector P20 (Hirose DF9B-31P-1V)

Important Note

Do not draw more than 1.0 Ampere from VCC_LCD (max. 0.5 Ampere per pin).

Device Connection (Inverter)

Mating connector type: Housing Molex 51021-0400, Crimp contact Molex 50058-8100.
Wiring: AWG26.

Pin Number	Signal	Remarks
1	VCC_INV	Inverter Power 5V
2	VCC_INV	Inverter Power 5V
3	GND	Ground
4	GND	Ground
5	EN	Inverter enable
6	LCD Brightness (0..5V)	Brightness Control
7	S2 Slider 1	Inverter Configuration input (off=open/on=ground)
8	S2 Slider 2	Inverter Configuration input (off=open/on=ground)

Tab. 10 Inverter connector P21 (Molex 53398-0871)

Important Note

Do not draw more than 2.0 Ampere from VCC_INV (max. 1.0 Ampere per pin).

3.3.4. IDE/CompactFlash-Interface

The IDE interface is setup as Primary IDE Channel with standard PC address decoding and using hardware interrupt 14. It supports 2 external devices on a single connection, one configured as master the other as slave. Alternatively one external device may be replaced by an on board pluggable CompactFlash card. The IDE timing is setup by software (BIOS autodetection). IDE interface activity is shown by a flashing yellow LED on the front side.
The IDE interface provides the following configuration options:

Configuration Options

Jumper	Configuration	Remarks
J1	Pin 2-4 open = on board CompactFlash is slave Pin 2-4 closed = on board CompactFlash is master	don't care if only external devices are connected.

Tab. 11 IDE Configuration Options

Device Connection

External IDE devices are connected through the standard 2x22 pin header J15. A CompactFlash card may be directly plugged in the on board CompactFlash connector P8.

Pin Number	Signal	Pin Number	Signal
1	RST*	2	GND
3	HD7	4	HD8
5	HD6	6	HD9
7	HD5	8	HD10
9	HD4	10	HD11
11	HD3	12	HD12
13	HD2	14	HD13
15	HD1	16	HD14
17	HD0	18	HD15
19	GND	20	nc (KEY)
21	DRQ	22	GND
23	HIOW*	24	GND
25	HIOR*	26	GND
27	IOCHRDY	28	GND
29	DACK*	30	GND
31	IRQ	32	IOCS16*
33	HA1	34	PDIAG*
35	HA0	36	HA2
37	HCS0*	38	HCS1*
39	DASP*	40	GND
41	VCC (5V)	42	VCC (5V)
43	GND	44	nc

Tab. 12 IDE Connector P7 (2x22 pin)

Important Notes

Do not connect 2 external devices and a CompactFlash card together. This may damage the system and the IDE devices.

3.3.5. Serial Ports

Two serial ports are available. The serial ports have fixed base addresses of 3F8H for COM1 and 2F8H for COM2. COM1 uses hardware interrupt 4 and COM2 uses hardware interrupt 3.

Device Connection

The Serial Port COM1 is available on the internal header P5.
The Serial Port COM2 is available on the internal header P6.

Pin Number	Signal	Pin Number	Signal
1	DCD*	2	DSR*
3	RXD	4	RTS*
5	TXD	6	CTS*
7	DTR*	8	RI*
9	GND	10	+5V (not fused)

Tab. 13 Serial Port COM1 and COM2 internal Headers P5, P6 (2x5 pin)

3.3.6. Keyboard/Mouse Interface

The keyboard signals are available on the MiniDIN connector P3 for direct connection of PS/2 style keyboards. The PS/2-mouse signals are available on the internal header P4. The controller uses hardware interrupt 1 for the keyboard and hardware interrupt 12 for the mouse. The following configuration options are provided:

Configuration Options

Jumper	Configuration	Remarks
P4	Pin 1-3, 2-4 closed = Keyboard signals on P3 Pin 3-5, 4-6 closed = Mouse signals on P3	

Tab. 14 Keyboard/Mouse Configuration Options

Device Connection

The standard PS/2 connector P3 is used for direct connection of the keyboard or mouse (depending on jumper configuration). The Keyboard/Mouse signals are also available on the internal 2x5 pin header P4 for connection of the other device. P3 is not available on NETIPC-4AD, use P4 instead.

Pin Number	Signal	Remarks
1	KBDATA / MDATA	
2	- (Boot Mode Pin BM1)	do not connect
3	GND	
4	+5V (not fused)	
5	KBCLK / MCLK	
6	- (Boot Mode Pin BM0)	do not connect

Tab. 15 Keyboard/Mouse connector P3 (PS/2)

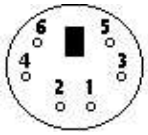

Fig. 4 6-pin female Mini-DIN (PS/2) socket (front view)

Pin Number	Signal	Pin Number	Signal
1	KBDATA	2	KBCLK
3	P3-1	4	P3-5
5	MDATA	6	MCLK
7	BM1 / P3-2	8	BM0 / P3-6
9	GND	10	+5V (not fused)

Tab. 16 Keyboard/Mouse internal Header P4 (2x5 pin)

Important Note

Do not connect the Boot Mode Pins on P3 or P4. These signals may only be used by the Boot Loader Key to start the Boot Loader.
The Boot Loader Key (BOOTPLUG) shortens Pin 3 and 6 of P3.

Important Note

Maximum cable length allowed for keyboard and mouse connection is 3 m.
Use shielded cables for maximum EMI protection.

3.3.7. USB Interface

The NETIPC-4A features an OHCI/EHCI compatible USB hostcontroller having assigned the base address and IRQ at boot time by the PCI-BIOS.

Device Connection

The USB interface uses two 4pin headers for the two USB channels.

P14 Pin Number	USB channel 0 Signal	P15 Pin Number	USB channel 1 Signal
1	VBUS	1	VBUS
2	D-	2	D-
3	D+	3	D+
4	GND	4	GND

Tab. 17 USB Interface Connector P14/P15 (1x4pin/1x4pin)

3.3.8. Ethernet Interface

The NETIPC-4A features a PCI Ethernet controller having assigned the base address and IRQ at boot time by the BIOS. The Ethernet interface drives two LED's (yellow and green) integrated into the RJ45 connector for status information. The meaning of the LED activity is programmable (normally set by the low level driver).
No configuration options are available for the Ethernet device.

Device Connection

The Ethernet interface uses the standard RJ45 connector P10 for 100Ω shielded or unshielded Twisted Pair cabling.

Pin Number	Signal	Remarks
1	TX+	
2	TX-	
3	RX+	
4-5	line termination	
6	RX-	
7-8	line termination	

Tab. 18 Ethernet Twisted Pair Interface Connector P10 (RJ45)

3.3.9. Watchdog

The watchdog timer is configurable for 100 ms or 1.6 s timeout. Once timed out, it may activate the NETIPC's hardware reset or the processors NMI line depending on software configuration.

Configuration Options

Jumper	Configuration	Remarks
J1	Pin 4-6 open = 1.6 s Pin 4-6 closed = 100 ms	

Tab. 19 Watchdog Configuration Options

3.3.10. PC/104 Bus Interface

The PC/104 bus interface of the NETIPC allows expansion with a wide range of I/O and communications boards. The bus interface is described in the IEEE 996 and 996.1 standards documentation. The bus connector pinout is shown in Tab. 20. For single board applications only the power pins should be connected. See paragraph 5.1 for electrical specification.

Pin		*Signal Name*	*Pin*		*Signal Name*	*Pin*		*Signal Name*	*Pin*		*Signal Name*
						A1	⊗	IOCHCK#	B1	⊗	GND
P11			P12			A2	⊗	SD7	B2	⊗	RESETDRV
1	⊗	GND	1	⊗	GND	A3	⊗	SD6	B3	⊗	+5V
2	⊗	no connection	2	⊗	+5V	A4	⊗	SD5	B4	⊗	IRQ9
3	⊗	no connection	3	⊗	TRIGGER*	A5	⊗	SD4	B5	⊗	-5V (not used)
4	⊗	Vbatt	4	⊗	STOP*	A6	⊗	SD3	B6	⊗	DRQ2
						A7	⊗	SD2	B7	⊗	-12V (not used)
						A8	⊗	SD1	B8	⊗	0WS#
D0	⊗	GND	C0	⊗	GND	A9	⊗	SD0	B9	⊗	+12V (not used)
D1	⊗	MEMCS16#	C1	⊗	SBHE#	A10	⊗	IOCHRDY	B10	⊗	(KEY)
D2	⊗	IOCS16#	C2	⊗	LA23	A11	⊗	AEN	B11	⊗	SMEMW#
D3	⊗	IRQ10	C3	⊗	LA22	A12	⊗	SA19	B12	⊗	SMEMR#
D4	⊗	IRQ11	C4	⊗	LA21	A13	⊗	SA18	B13	⊗	IOW#
D5	⊗	IRQ12	C5	⊗	LA20	A14	⊗	SA17	B14	⊗	IOR#
D6	⊗	IRQ15	C6	⊗	LA19	A15	⊗	SA16	B15	⊗	DACK3#
D7	⊗	IRQ14	C7	⊗	LA18	A16	⊗	SA15	B16	⊗	DRQ3
D8	⊗	DACK0#	C8	⊗	LA17	A17	⊗	SA14	B17	⊗	DACK1#
D9	⊗	DRQ0	C9	⊗	MEMR#	A18	⊗	SA13	B18	⊗	DRQ1
D10	⊗	DACK5#	C10	⊗	MEMW#	A19	⊗	SA12	B19	⊗	REFRESH#
D11	⊗	DRQ5	C11	⊗	SD8	A20	⊗	SA11	B20	⊗	SYSCLK
D12	⊗	DACK6#	C12	⊗	SD9	A21	⊗	SA10	B21	⊗	IRQ7
D13	⊗	DRQ6	C13	⊗	SD10	A22	⊗	SA9	B22	⊗	IRQ6
D14	⊗	DACK7#	C14	⊗	SD11	A23	⊗	SA8	B23	⊗	IRQ5
D15	⊗	DRQ7	C15	⊗	SD12	A24	⊗	SA7	B24	⊗	IRQ4
D16	⊗	+5V	C16	⊗	SD13	A25	⊗	SA6	B25	⊗	IRQ3
D17	⊗	MASTER#	C17	⊗	SD14	A26	⊗	SA5	B26	⊗	DACK2#
D18	⊗	GND	C18	⊗	SD15	A27	⊗	SA4	B27	⊗	TC
D19	⊗	GND	C19	⊗	(KEY)	A28	⊗	SA3	B28	⊗	BALE
						A29	⊗	SA2	B29	⊗	+5V
						A30	⊗	SA1	B30	⊗	OSC
						A31	⊗	SA0	B31	⊗	GND
						A32	⊗	GND	B32	⊗	GND

Tab. 20 PC/104 Bus Connectors PA/PB, PC/PD

Important Note

For proper operation ***all*** +5V and GND pins must be connected with short, low impedance lines to the main power supply.

The NETIPC board is not fully IEEE 996.1 (PC/104) compliant. The following restrictions and differences to the IEEE 996.1 specification apply:

- connector and mounting holes are compatible but the board dimensions are bigger (100 x 120 mm^2)
- The interrupt lines are pulled up with 8k2 resistors to Vcc (EISA specification) instead of 2k2 (IEEE 996)

Important Note

Do not connect bus drivers/receivers with integrated bushold circuit to the PC/104 signals. This may disturb proper operation of the NETIPC board or add-on boards.

3.3.11. Frontside Status LEDs

The three colored LEDs on the front side show the following states:
Green LED - Board ready (programming see Setup register in chapter 4)
Yellow LED - IDE interface activity (hard disk or CompactFlash)
Red LED - STOP signal (programming see Control register in chapter 4)

4 Programming Information

4.1. Overview

The programming of the NETIPC board is done with standard memory and I/O read and write operations. Most configuration options are handled by the BIOS. For detailled information refer to the NETIPC firmware documentation and other related documents as listed in paragraph 1.3.
Please contact Syslogic technical support if you need special BIOS configuration.

4.2. Interrupt, Memory and I/O Resources

4.2.1. Interrupt Resources

The following table shows the usage of the NETIPC's interrupt inputs. Interrupts marked 'shared' are shared between an onboard device and an FBCube bus interrupt line. These interrupts should only be used for multiple interrupt sources, if all interrupt routines are able to process shared interrupts (normally not the case for keyboard, COM1/2, Ethernet, Mouse and IDE interrupt drivers). Interrupts marked 'free' are not used by onboard devices if they are not assigned to a PCI device in the BIOS configuration.

Interrupt	Interrupt Source	Remarks
Master		
IRQ0	Timer Channel 0	
IRQ1	Keyboard	
IRQ2	Slave Interrupt Controller Cascading	
IRQ3	COM2	shared
IRQ4	COM1	shared
IRQ5	PC/104 Bus IRQ5	free
IRQ6	PC/104 Bus IRQ6	free
IRQ7	PC/104 Bus IRQ7	free (PCI-USB)
Slave		
IRQ8	Real Time Clock	
IRQ9	PC/104 Bus IRQ9	free (PCI-VGA)
IRQ10	Ethernet Controller	do not connect
IRQ11	PC/104 Bus IRQ11	free
IRQ12	PS/2-Mouse	
IRQ13	Floating Point Unit	
IRQ14	Primary IDE Channel	do not connect
IRQ15	PC/104 Bus IRQ15	free
Special		
NMI	Watchdog and PC/104 Bus Error Interrupt IOCHCK*	shared

Tab. 21 Interrupt Usage

4.2.2. Memory Resources

The general memory layout is shown in paragraph 3.2.1. The configuration of the memory layout is done by programming processors internal configuration registers and board configuration registers (see paragraph 4.2.3). This is done completely by the BIOS on system startup and must not be changed during operation. For operating systems requiring memory configuration (e.g. Windows CE) the memory layout shown in paragraph 3.2.1 must be considered.

4.2.3. I/O Resources

This paragraph describes only the NETIPC system register and support functions not directly related to a specific peripheral device. The general I/O layout is shown in paragraph 3.2.2. Peripheral devices are discussed in paragraph 4.3. Note that the Socket Memory related registers are programmed by the BIOS on system startup and must not be changed during operation except for the Socket Memory Window Mapping Register in case of user controlled memory mapping (allowing access to 512kbyte Socket Memory as eight 64kbyte blocks in the Socket Memory window below 1M in Real Mode).

Address	Device / Register	Remarks
8200H	Status Register	
8201H	Control Register	Reset state = 05H
8202H	Function ID Register	
8203H	reserved	do not write
8204H	Option ID Register	
8205H	Setup Register	Reset state = 00H
8206H	Revision ID Register	
8207H	Socket Memory Configuration Register	Reset state = 00H
8208H	Socket Memory Window Mapping Register	Reset state = 00H
8209H	Socket Memory Window Base Address Register	Reset state = D0H
820AH	Boot Mode Input Register	
820BH	I2C Register	for Temp Sensor
820C..821FH	reserved	do not access

Tab. 22 NETIPC System Registers

Status Register

Reading I/O Register 8200H:

D7	D6	D5	D4	D3	D2	D1	D0
OVERTMP*	LOBAT*	1	WDG*	ERRFLAG*	ATTFLAG*	ERRINT*	ATTINT*

Description:

- ATTINT*: Attention Interrupt Status
  not used, returns 1
- ERRINT*: Error Interrupt Status
  0 = Error Interrupt pending on this module
  1 = no Error Interrupt pending on this module
- ATTFLAG*: Attention Status Flag (for polled applications)
  not used, returns 1
- ERRFLAG*: Error Status Flag (for polled applications)
  not used, returns 1
- WDG*: Watchdog Status Flag
  0 = Watchdog has timed out
  1 = Watchdog running or disabled
  Reset by issuing a hardware reset (see register 8204H)
- LOBAT*: Battery Status Flag
  0 = Battery voltage low
  1 = Battery voltage ok
- OVERTMP*: Temperatur Sensor Status Flag
  0 = programmed temperatur limit reached
  1 = temperatur ok (below limit)

Writing I/O Register 8200H:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Description:

- reserved: reserved, always write 0

Control Register

Reading I/O Register 8201H:

D7	D6	D5	D4	D3	D2	D1	D0
TRIG*	WDTRIG	WDNMI	STOP	TRIGSRC	FREEZE	ERREN*	ATTEN*

Description:

- ATTEN*: Attention Interrupt Enable
  not used, returns 1
- ERREN*: Error Interrupt Enable (IOCHCK* routed to NMI)
  0 = Error interrupt on NMI enabled (always enabled)
- FREEZE: not used, returns 1
- TRIGSRC: NETIPC TRIGGER* Signal Source Select
  0 = hardware timer (see Tab. 23)
  1 = software timer (see Tab. 23)
- STOP: NETIPC STOP* Signal State (see remarks below)
  0 = STOP* inactive (high)
  1 = STOP* active (low)
- WDNMI: Watchdog action Select
  0 = Watchdog timeout activates hardware reset
  1 = Watchdog timeout activates Non Maskable Interrupt
- WDTRIG: Watchdog Trigger
  any state change triggers the watchdog (timeout reset)
- TRIG*: Direct Control for NETIPC TRIGGER* Signal (see remarks below)
  0 = TRIGGER* Signal low
  1 = TRIGGER* Signal high

Writing I/O Register 8201H:

D7	D6	D5	D4	D3	D2	D1	D0
TRIG*	WDTRIG	WDNMI	STOP	TRIGSRC	FREEZE	ERREN*	ATTEN*

Description:

- ATTEN*: Attention Interrupt Enable
  not used
- ERREN*: Error Interrupt Enable (IOCHCK* routing to NMI)
  0 = enable Error interrupt on NMI (always enabled)
- FREEZE: not used
- TRIGSRC: NETIPC TRIGGER* Signal Source Select
  0 = hardware timer (see Tab. 23)
  1 = software timer (see Tab. 23)
- STOP: NETIPC STOP* Signal State
  0 = STOP* inactive (high)
  1 = STOP* active (low)
- WDNMI: Watchdog action Select
  0 = Watchdog timeout activates hardware reset
  1 = Watchdog timeout activates Non Maskable Interrupt

- WDTRIG: Watchdog Trigger
  any state change triggers the watchdog (timeout reset)
- TRIG*: Direct Control for NETIPC TRIGGER* Signal
  (if enabled by TRIGSRC bit in Control Register)
  0 = TRIGGER* Signal low
  1 = TRIGGER* high

TRIGSRC	TRIG*	TRIGGER* Source
0	0	*reserved* for Square Wave Output (SQW) of Real Time Clock Device
0	1	Timer (8254) Channel 2 Output gated with Port B bit 1 (Speaker Enable)
1	X	TRIG* bit directly controls the TRIGGER* output

Tab. 23 TRIGGER* Source Selection

The STOP* and TRIGGER* signals are intended for control of add-on boards. Both signals are available on the PC/104 bus connector extension P12.

STOP* is intended as signal to force an add-on board function to a specified state. For example with the digital I/O board IPC/DIO32 the STOP* signal is used to either reset or freeze the state of the digital outputs depending on setup of the DIO32 board as long as the STOP* signal is active (low).
The STOP* signal also directly drives the red LED on the front (STOP* low = LED on).
Upon startup STOP* is active (LED on) until the BIOS has initialized the main peripherals, it is set inactive (LED off) before booting the operating system. STOP* is also active (LED on) while operating in Bootloader mode.

TRIGGER* is intended as a signal to synchronize operations on add-on boards controlled by software or by a fix frequency.
Alternately TRIGGER* may carry the speaker output to an add-on board for control of a buzzer.

Important Note
The SQW trigger source is not supported on NETIPC-4A/-4AD.

Function ID Register

Reading I/O Register 8202H:

D7	D6	D5	D4	D3	D2	D1	D0
FID7	FID6	FID5	FID4	FID3	FID2	FID1	FID0

Description:

- FID7..0: Function ID
  0101'0001 (51H) = general NETIPC board,
  subtype defined by Option ID Register

Writing I/O Register 8202H:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Description:

- reserved: reserved, always write 0

Option ID Register

Reading I/O Register 8204H:

D7	D6	D5	D4	D3	D2	D1	D0
OPT7	OPT6	OPT5	OPT4	OPT3	OPT2	OPT1	OPT0

Description:

- OPT7..0: Option ID
  1000'0101 (89H) = IPC/NETIPC-4A/-4AD version (if FID = 51H)

Writing I/O Register 8204H:

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X

Description:

- xxxxxxxx: Writing data A5H invokes a complete hardware reset (also clearing the Watchdog timeout status bit)

Setup Register

Reading I/O Register 8205H:

D7	D6	D5	D4	D3	D2	D1	D0
READY	WDEN	0	0	0	0	0	0

Description:

- WDEN: Watchdog Enable
  0 = Watchdog disabled
  1 = Watchdog enabled (running)
- READY: NETIPC READY Signal State
  0 = READY inactive
  1 = READY active

Writing I/O Register 8205H:

D7	D6	D5	D4	D3	D2	D1	D0
READY	WDEN	reserved	reserved	reserved	reserved	reserved	reserved

Description:

- reserved: reserved, always write 0
- WDEN: Watchdog Enable
  0 = Watchdog disabled (cannot be disabled while running)
  1 = enable Watchdog
- READY: NETIPC READY Signal State
  0 = deactivate READY
  1 = activate READY

The READY* signal directly drives the green LED on the front (READY* low = LED on).
Upon startup READY* is inactive (LED off) until the BIOS has initialized the main peripherals, it is set active (LED on) before booting the operating system. READY* is also inactive (LED off) while operating in Bootloader mode.
On NETIPC –1A, -2A and –3A board variants, READY* also drives the reset line of the Ethernet controller (READY* high = Ethernet controller in reset state). Therefore READY* should not be deactivated by the operating system or application software. Always read back the current state before programming this setup register for enabling the watchdog!

Revision ID Register

Reading I/O Register 8206H:

D7	D6	D5	D4	D3	D2	D1	D0
RID7	RID6	RID5	RID4	RID3	RID2	RID1	RID0

Description:

- RID7..0: Revision ID
  xxH = Logic Design revision ID (see Product Revision History)

Writing I/O Register 8206H:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Description:

- reserved: reserved, always write 0

Socket Memory Configuration Register

Reading I/O Register 8207H:

D7	D6	D5	D4	D3	D2	D1	D0
SOCKEN	0	0	0	0	0	0	MSIZE

Description:

- MSIZE: Socket Memory Window Size (below 1 M)
  0 = 32 kbyte
  1 = 64 kbyte
- SOCKEN: Socket Memory Window Enable
  0 = Window disabled below 1 M
  1 = Window enabled below 1 M

Writing I/O Register 8207H:

D7	D6	D5	D4	D3	D2	D1	D0
SOCKEN	0	0	0	0	0	0	MSIZE

Description:

- MSIZE: Socket Memory Window Size (below 1 M)
  0 = 32 kbyte
  1 = 64 kbyte
- SOCKEN: Socket Memory Window Enable
  0 = disable Window below 1 M
  1 = enable Window below 1 M

Socket Memory Window Mapping Register

Reading I/O Register 8208H:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	MMR2	MMR1	MMR0

Description:

- MMR2..0: Socket Memory Window Mapping Bit 2..0
  enables mapping of eight 64 kbyte pages (= 512 kbyte)

Writing I/O Register 8208H:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	MMR2	MMR1	MMR0

Description:

- MMR2..0: Socket Memory Window Mapping Bit 2..0
  enables mapping of eight 64 kbyte pages (= 512 kbyte)

Socket Memory Window Base Address Register

Reading I/O Register 8209H:

D7	D6	D5	D4	D3	D2	D1	D0
1	1	MBAS5	MBAS4	MBAS3	MBAS2	MBAS1	MBAS0

Description:

- MBAS7..0: Socket Memory Window Base Address Bit 19..12
  range C0000..E8000H

Writing I/O Register 8209H:

D7	D6	D5	D4	D3	D2	D1	D0
1	1	MBAS5	MBAS4	MBAS3	MBAS2	MBAS1	MBAS0

Description:

- MBAS7..0: Socket Memory Window Base Address Bit 19..12
  range C0000..E8000H

Boot Mode Input Register

Reading I/O Register 820AH:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	BM1	BM0

Description:

- BM1..0: Boot Mode Inputs
  0 = reserved (Factory Diagnostic Mode)
  1 = reserved
  2 = Boot Loader Mode
  3 = normal Operating Mode

Writing I/O Register 820AH:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Description:

- reserved: reserved, do not write

I2C Register (for temperatur sensor control)

Reading I/O Register 820BH:

D7	D6	D5	D4	D3	D2	D1	D0
SCLO	SDAO	SCL	SDA	1	1	1	1

Description:

- SDA: Data Port Pin State
  0 = Pin State = Low
  1 = Pin State = High
- SCL: Clock Port Pin State
  0 = Pin State = Low
  1 = Pin State = High
- SDAO: Data Port Output Latch State
  0 = Output Latch State = Low
  1 = Output Latch State = High (Open Collector)
- SCLO: Clock Port Output State
  0 = Output Latch State = Low
  1 = Output Latch State = High (Open Collector)

Writing I/O Register 820BH:

D7	D6	D5	D4	D3	D2	D1	D0
SCLO	SDAO	X	X	X	X	X	X

Description:

- SDAO: Data Port Output Latch
  0 = Output Latch State = Low
  1 = Output Latch State = High (Open Collector)
- SCLO: Clock Port Output
  0 = Output Latch State = Low
  1 = Output Latch State = High (Open Collector)

4.3. Peripheral Devices

4.3.1. VGA/LCD-Interface

The VGA interface uses the standard PC/AT VGA register set. For detailled programming information please refer to the IBM PC/AT Technical Reference or similar documentation.
Low level programming is handled by the VESA compatible VGA-BIOS.
The interface is built using the SiliconMotion SM712 (LynxEM4+) controller. For detailled programming information and drivers check www.syslogic.ch and www.siliconmotion.com .
For custom LCD BIOS requirements please contact Syslogic technical support.
This interface is not available on NETIPC-4AD.

4.3.2. IDE-Interface

The IDE interface uses the standard PC/AT register set. For detailled programming information please refer to the IBM PC/AT Technical Reference, ATA/ATAPI standards (ANSI) or similar documentation.

4.3.3. Serial Ports

The Serial Port interfaces use the standard PC/AT register set. The Serial Port controller is compatible with the standard 16C550A UART with 16 byte receive and transmit fifos. For detailled programming information please refer to the IBM PC/AT Technical Reference, the Texas Instruments TL16C550C datasheet or similar documentation.

4.3.4. Keyboard/Mouse Interface

The Keyboard/Mouse interface uses the standard PC/AT register set. The keyboard controller is compatible with the standard Intel 8042 device with integrated keyboard host controller firmware. For detailled programming information please refer to the IBM PC/AT and PS/2 Technical Reference, the Intel 82C42PC datasheet or similar documentation.

4.3.5. Ethernet Interface

On the NETIPC-4A board the Ethernet interface uses the RDC R6040 Ethernet Controller. For detailled programming information and drivers check www.syslogic.ch and www.dmp.com.tw.

4.3.6. USB Interface

The USB interfaces use the standard OHCI/EHCI register set. Legacy support and low level programming is handled by the BIOS and standard OS drivers.

4.3.7. Temperatur Sensor

The Temperator Sensor is built up using an LM75 compatible temperatur sensor programmable through an I2C interface. The I2C interface programming is done through the I2C Register of the NETIPC. For detailled programming information please refer to the National Semiconductor LM75 datasheet or similar documentation.
Poweron default setting for OVERTMP* is 80°C chip temperature.

4.3.8. Watchdog

The watchdog is disabled by default on poweron and must be enabled either by the BIOS or by the application program.
If watchdog programming is done from application software level, before enabling the watchdog by setting the WDEN bit in the NETIPC Setup Register, the watchdog action (RESET or NMI) must be programmed in the NETIPC Control Register (bit WDNMI).
If RESET activation is selected, the watchdog generates a hardware reset if it is not triggered within the configured timeout window by writing the WDTRIG bit in the NETIPC Control Register. The application must check the WDG* bit in the NETIPC Status Register uppon startup to identify the Watchdog as the source of the reset, and it must issue a hardware reset (by writing the value 0a5h to the NETIPC Option ID Register) to clear the WDG* flag. Otherwise the system resets again as soon as the Watchdog is started.
If NMI activation is selected, the watchdog generates a Non Maskable Interrupt to the processor if it is not triggered within the configured timeout window by writing the WDTRIG bit in the NETIPC Control Register. Note that enabling the NMI input of the processor also requires setting bit 7 of I/O port 70h (NMI mask) and clearing bit 3 of I/O port 61h (Port B IOCHK# enable). The NMI routine must check the WDG* bit in the NETIPC Status Register to identify the watchdog as the source of the NMI, and it must issue a hardware reset (by writing the value 0a5h to the NETIPC Option ID Register) to clear the WDG* flag. Otherwise the NMI routine is entered again as soon as the watchdog is started.
Sample code showing the initialisation and triggering of the watchdog is available for RESET and NMI mode in the free IPC/IOCOMSW-1A package.

Note

The NMI mask bit (bit 7 of I/O port 70h) is write only. Typically it is enabled by the BIOS and should not be disabled by application software.

4.3.9. PC/104 Bus Interface

For detailed description of PC/104 add-on board programming please consult PC/104 and ISA bus standard documentation and related PC/AT architecture literature as well as the add-on boards documentation.

5 Technical Data

5.1. Electrical Data

Important Note

Do not operate the NETIPC board outside of the recommended operating conditions. Otherwise lifetime and performance will degrade. Operating the board outside of the absolute maximum ratings may damage the hardware.

Absolute Maximum Ratings (over free-air temperature range)

Parameter	Symbol	min	nom	max	Unit
internal power supply voltage	Vcc	-0.5		5.5	Vdc
isolation logic to chassis (AC, 60s, 500m a.s.l., Ta=25°C)		500			Vrms
isolation RJ45 to logic (AC, 60s, 500m a.s.l., Ta=25°C)		1500			Vrms
isolation RJ45 to chassis (AC, 60s, 500m a.s.l., Ta=25°C)		1000			Vdc
creepage distances:					
logic to chassis and PCB boarder		1.0			mm
logic to PC/104 mounting holes		0.5			mm
RJ45 to logic		2.5			mm
RJ45 to chassis and PCB boarder		2.0			mm
storage temperature range	Tst	-40		90	°C

Tab. 24 General Absolute Maximum Ratings

Recommended Operating Conditions

Parameter	Symbol	min	nom	max	
internal logic supply voltage	Vcc	4.75	5.00	5.25	Vdc
battery backup voltage (Io=100µA)	Vbatt	2.7	3.0	3.3	Vdc
PS/2 connector (P3/P4) power load (+5V)	Ips2			200	mA
operating free-air temperature range (standard products)	Ta	0		70	°C
operating free-air temperature range (extended range products IPC/NETIPC–xxE)	Ta	-40		85	°C

Tab. 25 General Recommended Operating Conditions

Electrical Characteristics
(over recommended operating range, unless otherwise noted)

Parameter	Symbol	min	typ	max	Unit
logic supply current (Vcc=5V, no external loads)	Icc		1.0	1.2	A
full load power dissipation (worst case)	Pmax		5.0	6.0	W
Vbatt loading (Vcc=0V, without SocketMemory)	Ibat(off)		2.5	27.5	uA
Vbatt loading (Vcc=5V)	Ibat(on)		1.5	4.0	uA
LOWBAT* trip point		2.35	2.5	2.65	V
VRT trip point (RTC Valid RAM and Time Flag)			1.3		V

Tab. 26 General Electrical Characteristics

Switching Characteristics
(over recommended operating range, unless otherwise noted)

Parameter	Symbol	min	nom	max	
processor clock (NETIPC-4A, -4AD)	pclk		800		MHz
processor clock (NETIPC-4AE, -4ADE)	pclk		600		MHz
UART base clock	fclk		1.8459		MHz
COM1/2 baud rate				115.2	kbaud
Watchdog timeout (short period)	Tw	70	100	140	ms
Watchdog timeout (long period)	Tw	1.0	1.6	2.25	s
Timer base clock	fclk		1.19318		MHz
Timer base clock accuracy				+/-100	ppm
Timer base clock aging				+/-5	ppm/year
Real Time Clock base clock	fclk		32.768		kHz
Real Time Clock accuracy (25°C)				+/-20	ppm
Real Time Clock temperature coefficient				-0.04	ppm/(°C)²
Real Time Clock aging				+/-3	ppm/year

Tab. 27 General Switching Characteristics

5.2. Mechanical Data

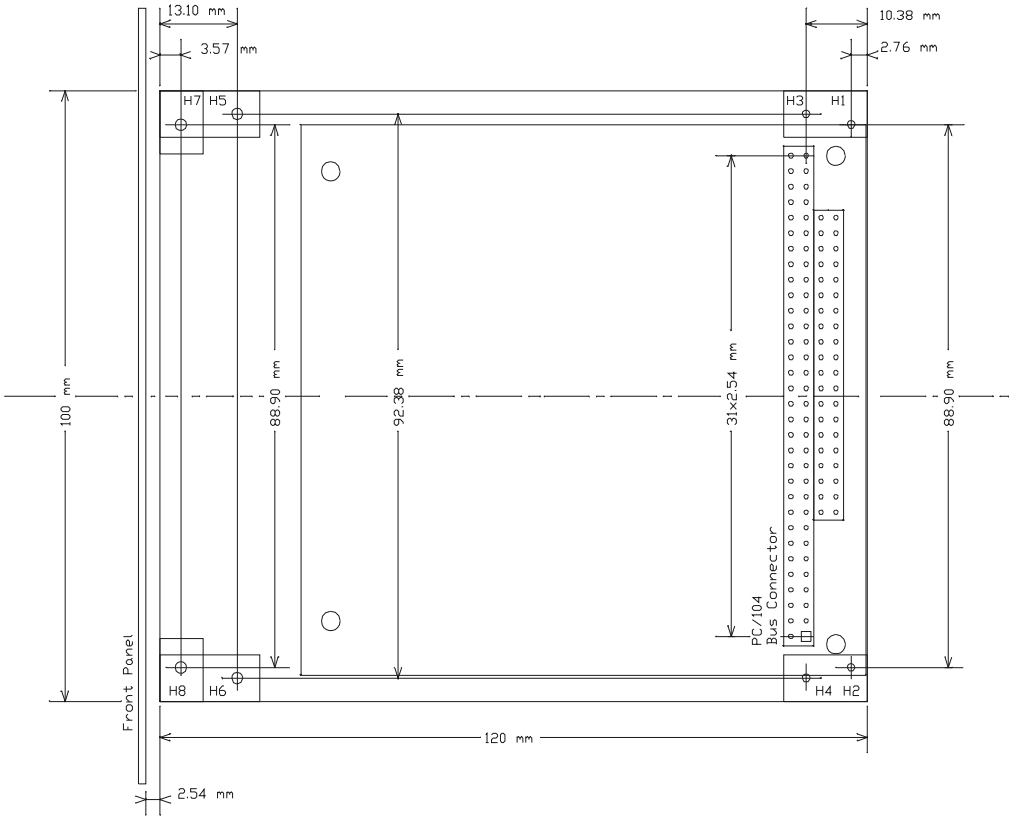

Fig. 5 Mechanical Outline

6 Firmware

6.1. Software Structure

The x86 CPU board based PC/104 system is based on the following software structure:

BIOS (Basic Input/Output System)

- Power On Self Test (POST)
- Initialization of standard peripheral devices
- Boot procedure for the Operating System

  Note : Refer to the BIOS documentation for detailled information

OS (Operating System)

- Initialization of additional peripheral devices
- Start procedure for the Application Programs

  Note : Refer to the OS documentation for detailled information

Application Programs

- Initialization of NETIPC system, communications and external devices
- Start procedure for the Control Tasks

  Note : Refer to the Application Programs documentation for detailled information

6.2. Firmware Functions

The NETIPC board is setup with BIOS firmware. Some standard PC/AT peripheral devices (e.g. VGA, Keyboard/Mouse, Serial Ports, IDE interface) are directly supported by the BIOS, BIOS extensions and Operating Systems. Some peripheral devices (e.g. Ethernet) are directly supported by standard communication software (e.g. TCP/IP stacks, TCP packet drivers) others need special programming according to the freely available sample software IPC/IOCOMSW-1A (e.g. Watchdog). Please refer to the appropriate documentation for detailled information.

6.3. Application Programming Interface (API)

The NETIPC board does not contain any special API beside the installed BIOS and DOS. Refer to the BIOS and Operating System documentation for API specifications.

7 Product Revision History

7.1. Hardware

This paragraph lists the different hardware revisions of the NETIPC boards delivered beginning with the first production lot. Note that prototyping boards are not included and must be returned to factory for upgrade or replacement. All information listed in this document relies on definitive state hardware. Therefore this information may be incompatible with the prototyping board hardware.

Board Identification (see product label)	Product Revision	Revision ID Register	Remarks
IPC/NETIPC-4A, -4AD #1	1	01H	Original Release
IPC/NETIPC-4AE, -4ADE #1	1	01H	Original Release

Tab. 28 Hardware Revision State

7.2. Hardware Erratas

This paragraph lists some important erratas of the current NETIPC boards to enable workarounds in user software. Additional erratas might be present but a workaround already implemented in the BIOS. It is important therefore that neither the application software nor the operating systems reprograms the processor chipset's configuration registers.
Note that prototype board erratas (boards with revision #0) are not listed here. Contact Syslogic technical support for prototype board information.

7.2.1. NETIPC-4A, -4AD Erratas

COM Port Receive Interrupt Bug (UART – universal asychronous receiver/transmitter)	
Problem	When the UART receive fifo is not empty and the UART is setup for reception, no interrupt is generated upon reception of additional characters. Then the receive fifo overruns.
Implication	No data received anymore.
Workaround 1	Always clear receive fifo before reenabling reception and always empty fifo completely upon receive interrupt.
Workaround 2	Disable fifo operation (16C450 mode).
Correction	This is a bug of the processor chip Vortex86DX. It will not be corrected. Use workaround.

7.3. Firmware

There is currently no errata information available.

Important Note

This document always covers the latest product revision listed in .
Please contact the manufacturers technical support for upgrade options.

8 Manufacturer Information

8.1. Contact

Our distributors and system integrators will gladly give you any information about our products and their use. If you want to contact the manufacturer directly, please send a fax or email message containing a short description of your application and your request to the following address or use one of the information or technical support request forms on our internet homepage:

Syslogic Datentechnik AG
Switzerland
Web: http://www.syslogic.ch
Email: info@syslogic.ch

Technical support:
support@syslogic.ch

8.2. Warranty

Our products are covered by a world-wide manufacturers warranty. The warranty period starts at the delivery time from our official distributor to the customer. The duration of the warranty period is specified in the respective product catalogs and the offers. All products carry a job number for identification. The manufacturing data and deliveries are registered in a high level Quality Management System.
The warranty covers material and manufacturing defects. All products must be returned via the official distributor to the factory for repair or replacement. The warranty expires immediately if the products are damaged of operation outside of the specified recommended operating conditions. The warranty also expires if the date code or job number listed on the product is altered or rendered unintelligible. The warranty does not include damage due to errors in firmware or software delivered with the products.